RF Circuit Performance Degradation Due to Soft Breakdown and Hot Carrier Effect in 0.18 μm CMOS Technology

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Abstract **A systematic study of RF circuit performance degradation subject to soft oxide breakdown (SBD) and hot carrier (HC) stress is demonstrated. Device parameters before and after stress are extracted from the experimental data of 0.18 mm CMOS technology. The effects of SBD and HC degradations on f_T, f_{max}, third-order interception point and the four noise parameters (F_{min}, R_n, G_{opt} and B_{opt}) of RF device have been studied. Since the figures of merit for the RF Circuit characterization are gain, noise figure, linearity and input matching, the RF Low noise amplifier performance drift is evaluated on these features. The predicted degradation trend from our experimental and simulation results can help design reliable CMOS RFICs.**

I. INTRODUCTION

Due to continued down scaling, deep submicron CMOS transistors offer the cutoff frequency (f_T) over 70 GHz and noise figure lower than 0.5 dB [1]. These features are more and more attractive for RF application up to 5 GHz [2,3]. CMOS technologies also offer low cost and high integration. However MOSFET HC and SBD induced device degradation poses a limit to the device scaling. Moreover the HC induced transistor aging and SBD induced degradation will seriously reduce the design margin of the RF circuit. It is important to evaluate the stress impact on the RF circuit performance to predict the time evolution.

This paper presents the soft oxide breakdown and hot carrier induced RF circuit performance degradation in 0.18 μm CMOS technology. The RF Circuit performance degradation of SBD and HC stressed CMOS circuit can be explained by the transconductance degradation, threshold voltage and mobility shift, which are result from the generation of phosphorous diffusion path in the gate oxide and the interface state generation (section II). Since the figures of merit for the RF device characterization are f_T, f_{max} and RF noise parameters (F_{min}, R_n, G_{opt} *and* B_{opt}). The effect of SBD and HC degradations has been studied on these features in section III. Based on the parameters extracted from 0.18 μm CMOS technology before and after stress, in section IV, CMOS RF Low noise amplifier is evaluated in terms of gain, noise figure, linearity and s-parameters in section IV .

II. HOT CARRIER AND SOFT BREAKDOWN EFFECT IN TRANSISTORS

Gate oxide breakdown and hot carrier effect are two critical issues of deep submicron CMOS reliability [4]. When the oxide is scaled down to 2 nm regime, soft breakdown would take place more often than hard breakdown (HBD); therefore SBD is being proposed as the failure criterion for new technologies. However, SBD has not been commonly recognized to degrade the device and circuit characteristics seriously. In this work we will present our experimental evidence of the impact of SBD, along with the hot carrier injection, on the RF circuits.

The devices used are 0.18 μm technology nMOSFETs. The gate width is 13.5 μm. The gate oxide thickness is 2.8 nm. The wafers are tested with the Cascade 12000 probe station and the HP 4156B precision semiconductor parameter analyzer. Oxide stress and channel hot carrier stress are applied to the transistor at the same time to mimic the real circuit operation condition while the source and drain are grounded. The hard breakdown voltage for this configuration is determined to be 5.7 V from voltage ramps. Then the accelerated stress condition is carefully set at $V_G = V_D = 5$ V. A very typical TDDB result is shown in Fig. 1. So many SBD events take place in both gate current and substrate current. We believe that the hot carrier injection triggers more soft breakdown occurrences. The drain current decreases due to the electron trapping and interface state generation and the degradation percentage goes up. Drain current showing considerable depress is given in Fig. 2. Electron trapping will cause the increase of threshold voltage. Interface state generation will decrease the electron mobility in the channel. The device parameters before and after the stress are extracted by virtue of BSIMpro [5]. The percentage degradation of Some important ones is summarized in Table I. All the parameters are transported into SPICE model files and are used to simulate the RF LNA with CADENCE SpectreRF.

TABLE I

PERCENTAGE OF BSIM3V3 DEVICE PARAMETER DEGRADATION

Parameters	V_{th0}	K_1	V_{sat}	μ_0	V_{off}	N-factor	P_{clm}
% change	11.7	100.2	-84	-68.8	163.3	-31.4	-96.8

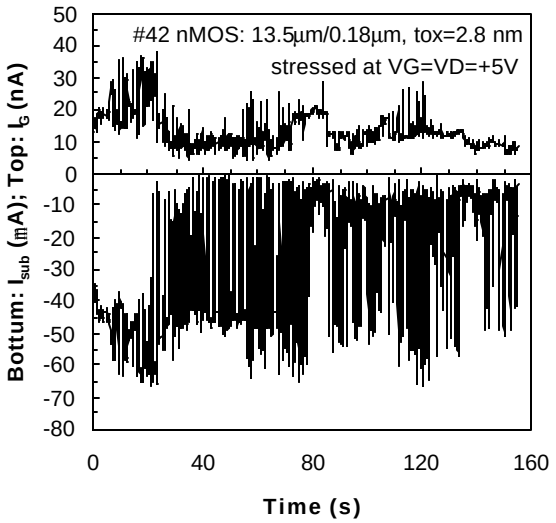

Fig. 1. TDDB result

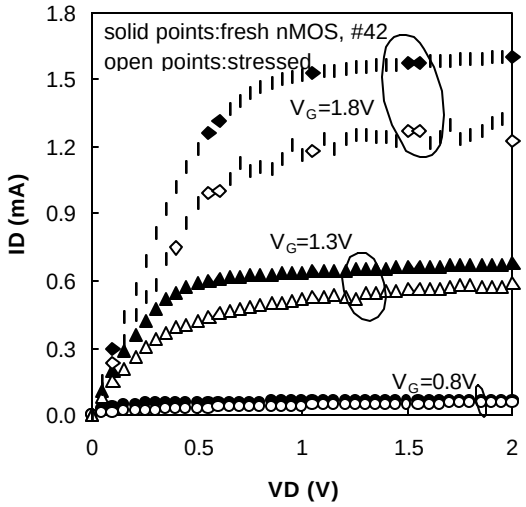

Fig. 2. Drain current depress after stress

III. DEGRADATION OF RF DEVICE CHARACTERIZATION

The most important parameters for high performance MOSFET at high frequencies are the gate resistance, threshold voltage, mobility transconductance and parasitic capacitances. The influence of these parameters on the unity short circuit current gain frequency f_T can be expressed as,

$$f_T = \frac{3}{2}\frac{\mu_{eff}}{L^2}(V_{gs}-V_T)\frac{L\varepsilon_{sat}+\frac{V_{gs}-V_T}{2}}{(L\varepsilon_{sat}+V_{gs}-V_T)^2} \qquad (1)$$

where $\varepsilon_{sat} = 2v_{sat}/\mu_{eff}$.

The maximum oscillation frequency f_{max} can be approximated by [6],

$$f_{MAX} \cong \sqrt{\frac{f_T}{8\pi R_g C_{gd}}} \qquad (2)$$

The noise performance of a linear front-end RF circuit is usually characterized by four noise parameters [7] as follows

$$NF = NF_{\min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2\right] \qquad (3)$$

where NF_{min} is the best performance that the circuit can achieve with the optimum source admittance condition ($G_s = G_{opt}, B_s = B_{opt}$), and R_n determines the sensitivity of NF when G_s and B_s differ from G_{opt} and B_{opt}. Expression for the four noise parameters (include the effect of gate resistance) are derived and summarized in Table II [8].

Also we expect input third-order intermodulation power P_{IIP3} grow according to (4)

$$P_{IIP3} = \frac{M^2}{2R_S} = \left|\frac{2A_1(s)}{3A_3(s_1,s_2,s_3)R_S}\right| \qquad (4)$$

where $A_1(s)$, $A_3(s_1,s_2,s_3)$ are Volterra series coefficients of the circuit, they are function of g_m, C_{gs}, ω_T, operation frequency ω, and circuit components (Lg, Ls and Rs) Values.

Table II

MOSFET noise parameters

Noise parameter	*Expression*
NF_{min}	$1+2\frac{f}{f_T}\sqrt{\frac{\delta(1-\lvert c\rvert^2)}{5}}\left[g'\left(1+\frac{f}{f_T}R_g g_m\right)^2+\frac{g_m^2}{g_{d0}}R_g\right]$
R_n	$\frac{g'g_{d0}}{g_m^2}(1+\omega C_{gs}R_g)^2+R_g$
G_{opt}	$\sqrt{\frac{\delta\omega^2 C_{gs}^2(1-\lvert c\rvert^2)}{5\frac{g'g_{d0}}{g_m^2}(1+\omega C_{gs}R_g)^2+5g_{d0}R_g}}$
B_{opt}	$\frac{\omega C_{gs}\sqrt{g'g_{d0}}}{\sqrt{g'g_{d0}(1+\omega C_{gs}R_g)^2+R_g g_m^2}}+\frac{g_m}{g_{d0}(1+\omega C_{gs}R_g)}\lvert c\rvert\sqrt{\frac{\delta}{5g'}}\omega C_{gs}$

Since g_m, C_{gs} and ω_T are degraded due to the interface state generation after SBD and HC stress, RF performances should be degraded due to the same degradation mechanism after hot carrier stress [9].

IV. RF CIRCUIT PERFORMANCE DEGRADATION

The goal of this research is to simulate the RF circuit performance degradation due to stress and help circuit designers design more reliable circuits. We evaluate the performance degradation of 2.45 GHz RF integrated low-noise amplifier. Some design guidelines are proposed for 0.18 µm CMOS RF Circuit.

Since the figure of merit for the characterization of RF circuit performance are noise figure (NF), gain, impedance matching (S_{11}) and linearity (third-order intermodulation point & 1dB compression point), these figures of merit are evaluated by using the parameters extracted from 0.18 µm device under stress condition. Fig. 3 is the schematic of RF LNA for 2.45 GHz single-chip CMOS transceiver. Differential architecture was selected for better rejection of common mode on-chip interference. Common-source input stage can get very low noise figure. Inductor L_g and on-chip spiral inductor L_s are used for impedance matching, while L_d is used to turn out the capacitance of following stage to get maximum power gain. Cascoded of the second stage can reduce the Miller effect and improve the output–input isolation.

In Fig. 3, The FET's are described by MOSFET RF model with BSIM3V3 core. The on chip spiral inductor is modeled by lumped component. Fig. 4 shows the s-parameters before and after stress.

The biasing for DC stress is V_{GS} = 5 V and V_{DS} = 5V. The stress time was 155 Seconds. From Fig. 4, S_{11} has been change significantly. The position of minimum has been moved away from the working frequency 2.45 GHz by 600 MHz after stress. At 2.45 GHz, S_{11} is degraded to -8dB from -27dB.

Among the RF performance degradation, noise figure degradation is most significant due to SBD. Since the fluctuations in the gate current directly cause noise at the gate electrode. Moreover, the resultant noise across the gate will casue drain-current fluctuations propotional to the gain of the device [10]. Fig. 5 shows the noise figure degradation of low noise amplifier due to stress. At 2.45GHz, the noise figure increased from 2 dB to 3 dB, which is unacceptable in the wireless receiver of most application.

Fig. 6 shows a plot of the voltage gain degradation. Voltage gain is reduced by 5 dB around center frequency.

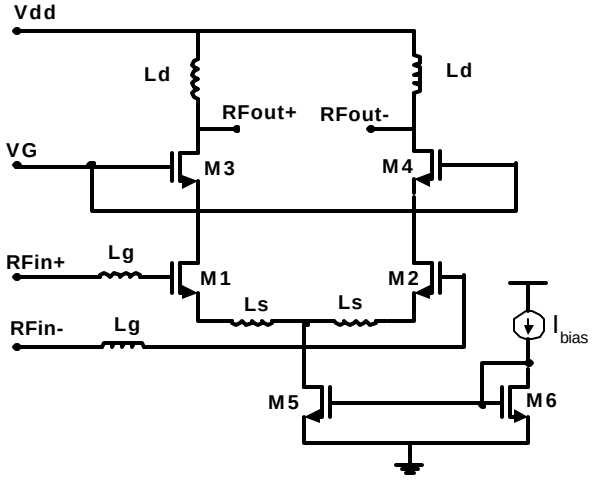

Fig. 3. Low noise amplifier for 2.45GHz CMOS transceiver

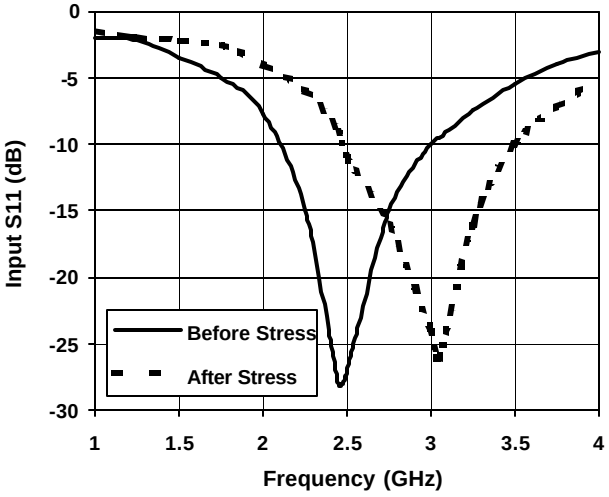

Fig.4 S-parameter before and after stress

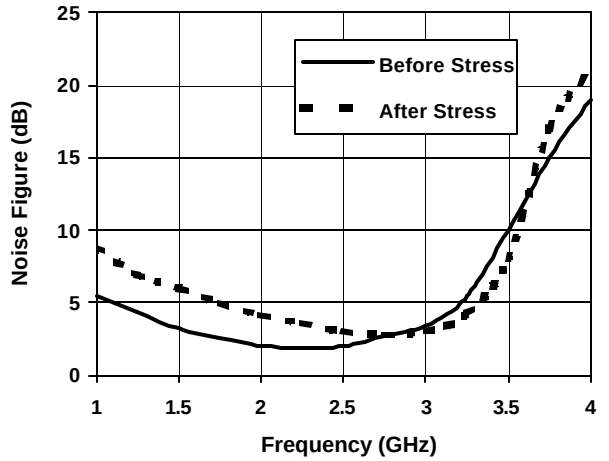

Fig. 5. Noise figure degradation

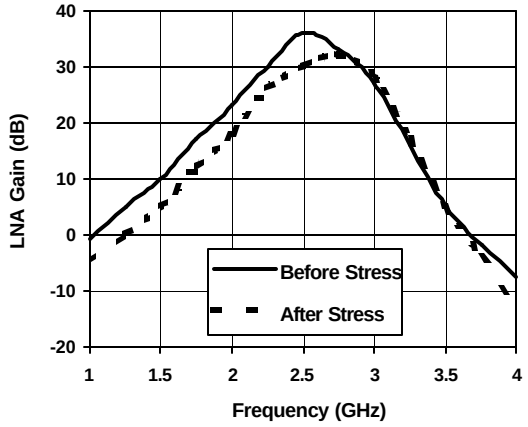

Fig. 6. Voltage gain degradation

Fig. 7 compares the output spectra of LNA before and after stress. The 3IM/1ST ratio of LNA before stress is -50 dBc. 3IM/1ST ratio of LNA after stress is -18 dBc. IIP3 is decreased by 16 dB after stress.

Table 3 summarizes the RF performance degradation of LNA under stress.

For the common-source input stage of LNA, the single-ended input impedance is

$$Z_{in} = \frac{1}{jwC_{gs}} + jw(L_s + L_g) + g_m \frac{L_s}{C_{gs}} \qquad (5)$$

From (5), the degradation of g_m and drift of C_{gs} after stress will change both the real part and imaginary part of the input impedance. The mismatch will cause the S_{11} shift away from the center frequency. The reason of noise figure degradation is because the degradation of f_T and the impedance deviation from the optimum value. From *Gain* = $Q_{in}g_mR_L$, both the degradation of the input stage Q_{in} and g_m can be attributed to the decrease of gain.

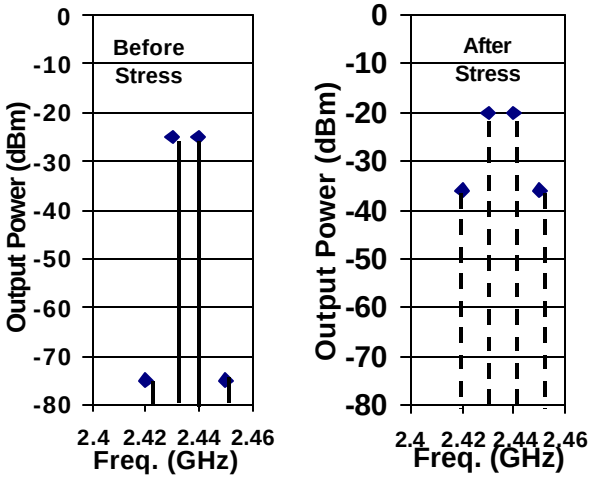

Fig. 7. Two tone simulation befroe and after stress

TABLE III
RF PERFORMANCE DEGRADATION OF LNA UNDER STRESS

Condition	*NF (dB)*	*Gain (dB)*	*IIP3 (dBm)*	*S_{11}(dB) 2.45GHz*
Before stress	2	36	-5	-27
After stress	3	31	-21	-9

V. CONCLUSION

The impact of SBD and HC on RF LNA was studied by stress actual on wafer FET in 0.18 μm CMOS Technology. BSIM3V3 model parameters were extracted based on the measurement before and after stress. The 2.45 GHz RF LNA was thoroughly investigated in terms of gain, noise figure, third-order intermodulation, and s-parameter. It was found SBD and HC effects seriously reduce the design margin of RF circuit with component transistor degradation. The predicted trend of performance degradation helps design reliable CMOS RFICs.

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